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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/731,060	12/07/2000	Edward Colles Nevill	550-192	1332
23117	7590 09/02/2004		EXAMINER	
NIXON & VANDERHYE, PC			ZHEN, LI B	
1100 N GLEBE ROAD 8TH FLOOR			ART UNIT	PAPER NUMBER
ARLINGTO	N, VA 22201-4714		2126	
			DATE MAILED: 09/02/2004	1

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)					
Office Action Summary	09/731,060	NEVILL ET AL.					
Onice Action Summary	Examiner	Art Unit					
The MAILING DATE of this communication app	Li B. Zhen	2126					
Period for Reply	ears on the cover sheet v	vian the correspondence address =					
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply if NO period for reply is specified above, the maximum statutory period of Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a within the statutory minimum of th will apply and will expire SIX (6) MC cause the application to become A	n reply be timely filed irty (30) days will be considered timely. NTHS from the mailing date of this communication. NBANDONED (35 U.S.C. § 133).					
Status							
1) Responsive to communication(s) filed on 20 M	<u>ay 2004</u> .						
2a) ☐ This action is FINAL . 2b) ☐ This action is non-final.							
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is							
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.							
Disposition of Claims							
4)⊠ Claim(s) <u>1-16</u> is/are pending in the application.							
4a) Of the above claim(s) is/are withdrawn from consideration.							
5) Claim(s) is/are allowed.							
6)⊠ Claim(s) <u>1-16</u> is/are rejected.							
7) Claim(s) is/are objected to.							
8) Claim(s) are subject to restriction and/o	r election requirement.						
Application Papers							
9)☐ The specification is objected to by the Examiner.							
10)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.							
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).							
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.							
	arriner. Note the attach	ou office Action of form 1.10 To 2.					
Priority under 35 U.S.C. § 119							
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).							
a) ☐ All b) ☐ Some * c) ☐ None of:							
1. Certified copies of the priority documents have been received.2. Certified copies of the priority documents have been received in Application No							
2. Certified copies of the priority document3. Copies of the certified copies of the priority							
application from the International Bureau		Troported in this realisma. Clays					
* See the attached detailed Office action for a list		ot received.					
		6					
Attachment(s)							
1) Notice of References Cited (PTO-892) Notice of Draftsperson's Patent Drawing Review (PTO-948) 4) Interview Summary (PTO-413) Paper No(s)/Mail Date							
3) Notice of Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) 5) Notice of Informal Patent Application (PTO-152)							
Paper No(s)/Mail Date <u>6/7/2004</u> . 6) Other:							

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DETAILED ACTION

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1. Claims 1 – 16 are pending in the application.

Information Disclosure Statement

2. The information disclosure statement filed March 31, 2004 and June 7, 2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

The reference, "A Pipeline Push-Down Stack Computer," is not legible, please resubmit a legible copy of the reference. Examiner was unable to locate some of the references cited in the IDS submitted on June 7, 2004 [p. 2], please resubmit a copy of the references. In addition, when citing excerpts from a book please specify page numbers.

Response to Arguments

3. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

;

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A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

- 5. Claims 1, 2, 7, 11 14 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent NO. 6,502,237 to Yates et al.
- 6. As to claim 1, Yates et al. teaches an apparatus [computer system 10, Fig. 1] for processing data operable to execute operations specified in a stream of program instructions [image stored in segment 17c corresponds to instructions which can be executed; col. 8, lines 29 39], the apparatus comprising:
- (i) a hardware based instruction execution unit operable to execute program instructions [the run-time system 32 can be implemented as... a hardware preprocessor to convert the non-native instructions into native instructions; col. 9, lines 52 67]; and
- (ii) a software based instruction execution unit [background process can be implemented in hardware or software or a combination of both; col. 11, lines 1-9] operable to execute program instructions [Translation into the native image is provided via a background system 34; col. 10, lines 60-67]; wherein
- (iii) program instructions to be executed are sent to the hardware based execution unit for execution [at the initiation of an execution of the program stored in segment 17b...the native loader 43 determines whether an architecture number

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associated with the non-native image indicates a native or a non-native image; col. 12, line 57 - col. 13, line 9];

- (iv) program instructions received by the hardware based execution unit for which execution is not supported by the hardware based execution unit are forwarded to the software based execution unit for execution [background system 34 receives the profile data generated by the run-time system 32. In accordance with the characteristics of the profile data, the background system 34 forms a native image of at least portions of the instructions of the non-native image; col. 11, lines 9 25] with control being returned to the hardware based execution unit for a next program instruction to be executed [If not then control is transferred to the interpreter. The interpreter continues to interpret and execute; col. 13, line 50 col. 14, line 3]; and
- (v) the hardware based execution unit includes scheduling support logic operable to generate a scheduling signal for triggering a scheduling operation to be performed between program instructions [Code scheduling typically rearranges sequences of instructions into a more optimal sequence due to resource contentions within the computer system 10; col. 78, line 63 col. 79, line 5; col. 79, lines 15 20] irrespective of whether a preceding program instruction was executed by the hardware based execution unit or the software based execution unit [server process 36 is a software service process which... is used to schedule various transactions within and between the run-time 32 and background systems 34; col. 11, lines 25 33].

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- 7. As to claim 16, this is a method claim that corresponds to apparatus claim 1; note the rejection to claim 1 above, which also meet this method claim.
- 8. As to claim 2, Yates et al. teaches the scheduling support logic includes a counter with a value [program counter...EIP; col. 16, lines 52 60] that is changed in response to a program instruction sent to the hardware based execution unit [col. 18, lines 30 34].
- 9. As to claim 7, Yates et al. teaches a debug operation is triggered by the scheduling signal [col. 72, lines 43 60].
- 10. As to claim 11, Yates et al. teaches a processor core operable to execute operations as specified by instructions of a first instruction set [col. 7, line 62 col. 8, line 5].
- 11. As to claim 12, Yates et al. teaches the hardware based instruction execution unit includes an instruction translator operable to translate instructions of a second instruction set into translator output signals corresponding to instructions of the first instruction set [profile statistics are used in a background process to convert portions of the non-native image into a native image corresponding to the operation and function of those portions of the non-native application program; col. 8, lines 39 49].

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- 12. As to claim 13, Yates et al. teaches (i) at least one instruction of the second instruction set specifies a multi-step operation that requires a plurality of operations that may be specified by instructions of the first instruction set in order to be performed by the processor core [col. 11, lines 10 25]; and
- (ii) the instruction translator is operable to generate a sequence of translator output signals to control the processor core to perform the multi-step operation [col. 8, lines 39 49].
- 13. As to claim 14, Yates et al. teaches the software based execution unit is a software based interpreter [run-time interpreter 44, Fig. 3; col. 12, lines 38 57].

Claim Rejections - 35 USC § 103

- 14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 15. Claims 3 6 and 8 10 are rejected over Yates et al. in view of applicant's admitted prior art [p. 2, hereinafter APA].
- 16. As to claim 3 6, Yates et al. does not specifically teach a counter that triggers generation of scheduling signal.

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However, APA states that it is known to control processing operations using a counter base approach whereby program instructions being executed are counted and a scheduling operation initiated each time a predetermined program instruction count level is reached [page 2, lines 12-15].

- 17. It would have been obvious to a person of ordinarily skilled in the art at the time of the invention to apply the teaching of a counter that triggers generation of scheduling signal as taught by APA to the invention of Yates et al. because this ensures that scheduling operations are stated at safe points between the execution of program instructions.
- 18. As to claim 8 10, Yates et al. as modified teaches timer based scheduling wherein a scheduling signal is combined with a timer signal to trigger scheduling [page 2, lines 15-17 of APA].
- 19. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yates et al.
- 20. As to claim 15, Yates et al. teaches the apparatus as claimed. However, Yates et al. does not teach that the program instructions are Java Virtual Machine instructions. Accordingly, it would have been obvious for one skilled in the art at the time the invention was made to implement the apparatus as claimed using Java Virtual Machine because an advantage of utilizing virtual machine instructions is that flexibility is

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achieved since the virtual machine instructions may be run, unmodified, on any computer system that has a virtual machine implementation, making for a truly portable language. Additionally, other programming languages may be compiled into Java virtual machine instructions and executed by a Java virtual machine.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Li B. Zhen whose telephone number is (571) 272-3768. The examiner can normally be reached on Mon - Fri, 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Li B. Zhen

Examiner

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SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2100

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lbz August 30, 2004